DECLARATION

I, the undersigned, of 16-1, Minamimukonoso 9-chome, Amagasaki-shi, Hyogo, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2000-253794**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

Masahiro Yamasaki

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Dated: **August 20, 2003**

[Name of the Document] Specification

[Title of the Invention] Semiconductor device and method for fabricating the same

[Claims]

[Claim 1] A semiconductor device characterized by comprising:

an insulating film formed on a substrate; and

an embedded wiring of copper or a copper alloy formed in the insulating film,

wherein a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the embedded wiring.

[Claim 2] A semiconductor device characterized by comprising:

an insulating film formed on a substrate; and

a wiring of copper or a copper alloy formed over the insulating film,

wherein a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the wiring.

[Claim 3] The semiconductor device of Claim 1 or 2, characterized in that the metal is Ru, Ir or an alloy containing Ru or Ir.

[Claim 4] The semiconductor device of Claim 1 or 2, characterized in that the metal oxide is RuO_2, IrO_2 or an alloy oxide containing Ru or Ir.

[Claim 5] A method for fabricating a semiconductor device, characterized by comprising the steps of:

forming a recess in an insulating film over a substrate;

sequentially depositing, over wall surfaces of the recess, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and a first conductive film of copper or a copper alloy;

growing a second conductive film of copper or a copper alloy on the first conductive film by an electroplating process so as to completely fill the recess; and

integrating the first conductive film and the second conductive film into a third conductive film so as to form an embedded wiring of the third conductive film.

[Claim 6] A method for fabricating a semiconductor device, characterized by comprising the steps of:

sequentially depositing, over an insulating film overlying a substrate, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and a first conductive film of copper or a copper alloy;

growing a second conductive film of copper or a copper alloy on the first conductive film by an electroplating process;

integrating the first conductive film and the second conductive film into a third conductive film; and

forming a wiring of the third conductive film by etching the third conductive film using a mask pattern covering a wiring forming region.

[Claim 7] A method for fabricating a semiconductor device, characterized by comprising the steps of:

forming a recess in an insulating film over a substrate;

depositing, on wall surfaces of the recess, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide; and

forming a conductive film of copper or a copper alloy on the barrier metal film so as to completely fill the recess and thereby forming an embedded wiring of the conductive film.

[Claim 8] A method for fabricating a semiconductor device, characterized by comprising the steps of:

depositing, on an insulating film overlying a substrate, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide;

forming a conductive film of copper or a copper alloy on the barrier metal film; and

forming a wiring of the conductive film by etching the conductive film using a mask pattern covering a wiring forming region.

[Claim 9] The semiconductor device fabrication method of Claim 7 or 8, characterized in that the conductive film is deposited by a sputtering process and then caused to flow in an oxidative-reducing atmosphere.

[Claim 10] The semiconductor device fabrication method of any one of Claims 5 to 8, characterized in that the metal is Ru, Ir or an alloy containing Ru or Ir.

[Claim 11] The semiconductor device fabrication method of any one of Claims 5 to 8, characterized in that the metal oxide is RuO_2, IrO_2 or an alloy oxide containing Ru or Ir.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a semiconductor device having a copper wiring and a method for fabricating the same.

[Prior Art]

With increase in operation speed of transistors, the delay due to CR components of wirings has become a matter of concern in silicon LSIs of 0.18 μm generation and the subsequent generations; therefore, an idea being studied is to use, instead of conventional Al (specific resistance of 3 μΩ • cm), Cu having a lower resistance (specific resistance of

1.7 μΩ • cm) or a metal primarily consisting of Cu (hereinafter, referred to as a "copper alloy") as a wiring material. Note that a wiring formed from copper or a copper alloy is herein referred to as a copper wiring.

Hereinafter, a conventional method for fabricating a semiconductor device will be described with reference to FIGS. **6**(a) through **6**(e) by taking, as an example, the copper wiring fabricating technology in which a Ta film (specific resistance of 200-230 μΩ • cm) is used as a barrier metal film.

First, as shown in FIG. **6(a)**, a first wiring **13** of a copper film is embedded in a first insulating film **11** on a semiconductor substrate **10** with a first barrier metal film **12** of a Ta film interposed therebetween. Thereafter, a first silicon nitride film **14**, a second insulating film **15**, a second silicon nitride film **16** and a third insulating film **17** are sequentially deposited over the semiconductor substrate **10**, and then a via hole **18** reaching the first wiring **13** is formed through the first silicon nitride film **14**, second insulating film **15** and second silicon nitride film **16**; in addition, a wiring trench **19** reaching the first wiring **13** through the via hole **18** is formed in the third insulating film **17**. In this case, the first barrier metal film **12** or the first silicon nitride film **14** prevents copper atoms constituting the first wiring **13** from diffusing into the first insulating film **11**, the second insulating film **15** or the like due to the thermal processing conducted at about 400°C for the deposition of the second insulating film **15**, the second silicon nitride film **16** or the like. In other words, the first barrier metal film **12** or the first silicon nitride film **14** serves as a barrier against diffusion of the copper atoms.

Then, as shown in FIG. **6(b)**, a second barrier metal film **20** of a Ta film and a copper seed layer **21** of a copper film are sequentially deposited over the bottoms and wall surfaces of the via hole **18** and the wiring trench **19** by a sputtering process.

The semiconductor substrate **10** is then transferred from the sputtering apparatus

into a plating apparatus. At this time, the surface of the semiconductor substrate **10**, i.e., the surface of the copper seed layer **21**, is exposed to the air. Then, as shown in FIG. **6(c)**, a copper plating film **22** is grown on the copper seed layer **21** by an electroplating process so as to completely fill the via hole **18** and the wiring trench **19**.

Thereafter, the copper plating film **22** is thermally processed (e.g., at a temperature of about 100°C for about two hours) in order to grow crystal grains of the copper plating film **22**. Thus, as shown in FIG. **6(d)**, the copper seed layer **21** and the copper plating film **22** are integrated into a wiring copper film **23**.

As shown in FIG. **6(e)**, parts of the second barrier metal film **20** and the wiring copper film **23** which are located outside the wiring trench **19** are then removed to form a via **24** and a second wiring **25** from the wiring copper film **23**. Thus, the first wiring **13** is connected to the second wiring **25** through the via **24**.

Although not shown, a desired multi-layer wiring structure is then formed as necessary by repeatedly conducting the steps shown in FIGS. **6(a)** through **6(e)** (regarding FIG. **6(a)**, the step of depositing the first silicon nitride film **14** and the subsequent steps).

[Problems that the Invention is to solve]

In the conventional fabrication method of the semiconductor device, however, the copper seed layer **21** deposited by the sputtering process might partially have a reduced thickness over the wall surface of the via hole **18** due to the directivity of the sputtering process, as shown in FIG. **7(a)**, and thus parts of the second barrier metal film **20** which are located on the wall surface of the via hole **18** might be exposed. As described before, the surface of the semiconductor substrate **10** is exposed to the air during transfer thereof from the sputtering apparatus into the plating apparatus after deposition of the copper seed layer **21**; thus, if the second barrier metal film **20**, i.e., the Ta film, has exposed parts at this time, those parts will be exposed to the air and therefore oxidized. In this case, the resultant Ta

oxide is a dielectric with very poor electric conductivity; accordingly, when the copper plating film **22** is grown by an electroplating process to fill the via hole **18**, an electric current does not flow through those oxidized parts of the second barrier metal film **20**. This might result in filling defects such as voids in the via hole **18** or the like as shown in FIG. 7 **(b)**. The similar problems are induced even when a TaN film (specific resistance of 200-230 μΩ • cm), a Ti film (specific resistance of 50 μΩ • cm) or a TiN film (specific resistance of 200 μΩ • cm), for example, is used as the second barrier metal film **20**.

Meanwhile, in order to fill a recess formed in the insulating film over the substrate with a copper film, a process such as a combination of sputtering and reflow processes, or a CVD (chemical vapor deposition) process may be used instead of the electroplating process.

Suppose that the combination of sputtering and reflow processes is used instead of the electroplating process and that an oxidation-reduction reflow process (Proc. of the 42nd Annual Meeting of JSAP (Spring, 1995), p. 810, Cu Wiring Technology (1) ~Reduced-Temperature Cu Reflow with Redox Cycle Reaction~) is used as the reflow process in the combination of sputtering and reflow processes. In that case, a thick copper film is deposited by a sputtering process over the insulating film in which the recess is formed with a barrier metal film of, e.g., a Ta film, interposed therebetween, the copper film is repeatedly oxidized and reduced in an oxidative-reducing atmosphere by an oxidation-reduction reflow process, and then the resultant reaction heat causes the copper film to flow, thereby filling the recess. However, when the copper film is oxidized, the conductivity of the barrier metal film is reduced due to the oxidation thereof, i.e., the oxidation of the Ta film or the like, and as a result, there arises the problem that the resistance of the wiring, the via or the like as well as the barrier metal film (which will be hereinafter simply referred to as "wiring resistance") might increase. The similar problem

is induced even when a copper film formed over the insulating film (which may have a recess therein) by the electroplating process, combination of sputtering and reflow processes, CVD process or the like is patterned into a wiring.

In view of the above, a first object of the present invention is to enable a conductive film to be formed on a seed layer or over a barrier metal film in a recess by an electroplating process, while preventing generation of filling defects, and a second object of the present invention is to prevent an increase in wiring resistance due to oxidation of the barrier metal film.

[Means for Solving the Problems]

In order to achieve the first and second objects, a first semiconductor device according to the present invention includes: an insulating film formed on a substrate; and an embedded wiring of copper or a copper alloy formed in the insulating film, wherein a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the embedded wiring.

In the first semiconductor device, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the embedded wiring. Thus, when a conductive film which will be the embedded wiring is formed by an electroplating process, the following effects can be achieved. Suppose that the barrier metal film and a seed layer are sequentially deposited over wall surfaces of a recess (a wiring trench, a via hole or the like) formed in an insulating film. In that case, even when the barrier metal film has exposed parts due to poor coverage of the seed layer, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, this enables the formation of the conductive film on the seed layer or over the barrier metal film located in

the recess by the electroplating process, while preventing generation of filling defects. Besides, when the conductive film which will be the embedded wiring is formed by some process other than an electroplating process, the following effects can be achieved. That is to say, when the barrier metal film is deposited on wall surfaces of the recess and then the conductive film is formed on the barrier metal film, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the barrier metal film will be lost due to the oxidation thereof. Thus, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

In order to achieve the second object, a second semiconductor device according to the present invention includes: an insulating film formed on a substrate; and a wiring of copper or a copper alloy formed over the insulating film, wherein a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the wiring.

In the second semiconductor device, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is formed between the insulating film and the wiring. Thus, when the barrier metal film is deposited on the insulating film and then the conductive film for the wiring is formed on the barrier metal film, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the barrier metal film will be lost due to the oxidation thereof. Thus, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

In the first or second semiconductor device, the metal is preferably Ru, Ir or an alloy containing Ru or Ir.

Thus, the barrier metal film can be reliably prevented from losing its conductivity due to the oxidation thereof.

In the first or second semiconductor device, the metal oxide is preferably RuO_2, IrO_2 or an alloy oxide containing Ru or Ir.

Thus, the barrier metal film can be reliably prevented from losing its conductivity due to the oxidation thereof.

In order to achieve the first object, a first method for fabricating a semiconductor device according to the present invention includes the steps of: forming a recess in an insulating film over a substrate; sequentially depositing, over wall surfaces of the recess, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and a first conductive film of copper or a copper alloy; growing a second conductive film of copper or a copper alloy on the first conductive film by an electroplating process so as to completely fill the recess; and integrating the first conductive film and the second conductive film into a third conductive film so as to form an embedded wiring of the third conductive film.

According to the first semiconductor device fabrication method, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and the first conductive film are sequentially deposited over wall surfaces of the recess formed in the insulating film over the substrate. Thereafter, the second conductive film is grown on the first conductive film by the electroplating process so as to completely fill the recess, and then the embedded wiring of the third conductive film into which the first conductive film and the second conductive film are integrated is formed. Suppose that the barrier metal film and the first conductive film, i.e., the seed layer, are sequentially deposited over wall surfaces of the recess. In that case, even when the barrier metal film has exposed parts due to poor coverage of the seed layer, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, this enables the formation of the second conductive film on the seed layer or

over the barrier metal film in the recess by the electroplating process, while preventing generation of filling defects.

In order to achieve the second object, a second method for fabricating a semiconductor device according to the present invention includes the steps of: sequentially depositing, over an insulating film overlying a substrate, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and a first conductive film of copper or a copper alloy; growing a second conductive film of copper or a copper alloy on the first conductive film by an electroplating process; integrating the first conductive film and the second conductive film into a third conductive film; and forming a wiring of the third conductive film by etching the third conductive film using a mask pattern covering a wiring forming region.

According to the second semiconductor device fabrication method, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide, and the first conductive film are sequentially deposited over the insulating film overlying the substrate. Thereafter, the second conductive film is grown on the first conductive film by the electroplating process, and then the third conductive film, into which the first conductive film and the second conductive film are integrated, is etched so as to form the wiring. Suppose that the barrier metal film and the first conductive film, i.e., the seed layer, are sequentially deposited over the insulating film. In that case, even when the barrier metal film has exposed parts due to poor coverage of the seed layer, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Thus, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

In order to achieve the second object, a third method for fabricating a semiconductor device according to the present invention includes the steps of: forming a

recess in an insulating film over a substrate; depositing, on wall surfaces of the recess, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide; and forming a conductive film of copper or a copper alloy on the barrier metal film so as to completely fill the recess and thereby forming an embedded wiring of the conductive film.

According to the third semiconductor device fabrication method, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is deposited on wall surfaces of the recess formed in the insulating film over the substrate, and then the conductive film is formed on the barrier metal film so as to completely fill the recess and to form the embedded wiring. Thus, when the barrier metal film is deposited on wall surfaces of the recess and then the conductive film is formed on the barrier metal film, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the barrier metal film will be lost due to the oxidation thereof. Therefore, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

In order to achieve the second object, a fourth method for fabricating a semiconductor device according to the present invention includes the steps of: depositing, on an insulating film overlying a substrate, a barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide; forming a conductive film of copper or a copper alloy on the barrier metal film; and forming a wiring of the conductive film by etching the conductive film using a mask pattern covering a wiring forming region.

According to the fourth semiconductor device fabrication method, the barrier metal film of a metal whose conductivity will not be lost even when the metal is oxidized or of a conductive metal oxide is deposited on the insulating film overlying the substrate, the

conductive film is formed on the barrier metal film, and then the wiring is formed by etching the conductive film. Thus, when the barrier metal film is deposited on the insulating film and then the conductive film is formed on the barrier metal film, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the barrier metal film will be lost due to the oxidation thereof. Therefore, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

In the third or fourth semiconductor device fabrication method, the conductive film is preferably deposited by a sputtering process and then caused to flow in an oxidative-reducing atmosphere.

Thus, the coverage of the conductive film is improved.

In the first, second, third or fourth semiconductor device fabrication method, the metal is preferably Ru, Ir or an alloy containing Ru or Ir.

Thus, the barrier metal film can be reliably prevented from losing its conductivity due to the oxidation thereof.

In the first, second, third or fourth semiconductor device fabrication method, the metal oxide is preferably RuO_2, IrO_2 or an alloy oxide containing Ru or Ir.

Thus, the barrier metal film can be reliably prevented from losing its conductivity due to the oxidation thereof.

[Embodiments of the Invention]

(First Embodiment)

Hereinafter, a semiconductor device and a fabrication method thereof according to the first embodiment of the present invention will be described with reference to FIGS. **1(a)** through **1(e)**.

First, as shown in FIG. **1(a)**, a first wiring **103** of, e.g., a copper film, is embedded in a first insulating film **101** on a semiconductor substrate **100** with a first barrier metal

film **102** of, e.g., a Ta film, interposed therebetween. Thereafter, a first silicon nitride film **104**, a second insulating film **105**, a second silicon nitride film **106** and a third insulating film **107** are sequentially deposited over the semiconductor substrate **100**, and then a via hole **108** reaching the first wiring **103** and having a depth of about 500 nm is formed through the first silicon nitride film **104**, second insulating film **105** and second silicon nitride film **106**; in addition, a wiring trench **109** reaching the first wiring **103** through the via hole **108** and having a depth of about 300 nm is formed in the third insulating film **107**. In this case, the first barrier metal film **102** or the first silicon nitride film **104** prevents copper atoms constituting the first wiring **103** from diffusing into the first insulating film **101**, the second insulating film **105** or the like due to the thermal processing conducted at about 400°C (e.g., plasma CVD process) for the deposition of the second insulating film **105**, the second silicon nitride film **106** or the like. In other words, the first barrier metal film **102** or the first silicon nitride film **104** serves as a barrier against diffusion of the copper atoms.

Next, as shown in FIG. **1(b)**, a second barrier metal film **110** of a Ru (ruthenium) film is deposited to a thickness of 25 nm over the semiconductor substrate **100** by, e.g., a sputtering process, and then a copper seed layer **111** of a copper film is deposited to a thickness of 150 nm on the second barrier metal film **110** by, e.g., a sputtering process. Thus, the bottoms and wall surfaces of the via hole **108** and the wiring trench **109** are covered with the second barrier metal film **110** and the copper seed layer **111**.

The semiconductor substrate **100** is then transferred from the sputtering apparatus into a plating apparatus. At this time, if the second barrier metal film **110** has exposed parts due to the poor coverage of the copper seed layer **111**, those parts will be exposed to the air and therefore oxidized. However, the specific resistance of Ru constituting the second barrier metal film **110** is 7.5 $\mu\Omega \cdot$ cm, while the specific resistance of RuO_2, which

is a Ru oxide, is 35 μΩ • cm; therefore, even when the second barrier metal film **110** is oxidized, the conductivity thereof will not be lost.

Then, as shown in FIG. **1(c)**, a copper plating film **112** is grown to a thickness of 500 nm on the copper seed layer **111** by an electroplating process so as to completely fill the via hole **108** and the wiring trench **109**. More specifically, after the semiconductor substrate **100** has been immersed in a plating solution including $CuSO_4$, H_2SO_4 and the like, the electroplating process is conducted such that the semiconductor substrate **100** has a negative potential. At this time, even if parts of the second barrier metal film **110** which are located on the wall surfaces of the via hole **108** or the like are not covered with the copper seed layer **111**, it is avoided that the conductivity of the second barrier metal film **110** will be lost due to oxidation thereof. Thus, the via hole **108** and the wiring trench **109** can be reliably filled with the copper plating film **112**.

Thereafter, the semiconductor substrate **100** is removed from the plating apparatus, and then the copper plating film **112** is thermally processed (e.g., at a temperature of about 100°C for about two hours) in order to grow crystal grains of the copper plating film **112**. As a result, the copper seed layer **111** and the copper plating film **112** are integrated into a wiring copper film **113** as shown in FIG. **1(d)**. Note that, instead of thermally processing the copper plating film **112** as described above, the semiconductor substrate **100** may be left to stand at room temperature for about two days.

As shown in FIG. **1(e)**, by a CMP process, for example, parts of the second barrier metal film **110** and the wiring copper film **113** which are located outside the wiring trench **109** are then removed to form a via **114** and a second wiring **115** from the wiring copper film **113**. Thus, the first wiring **103** is connected to the second wiring **115** through the via **114**.

Although not shown, a desired multi-layer wiring structure is then formed as

necessary by repeatedly conducting the steps shown in FIGS. **1(a)** through **1(e)** (regarding FIG. **1(a)**, the step of depositing the first silicon nitride film **104** and the subsequent steps).

As described above, according to the first embodiment, the second barrier metal film **110** of Ru, i.e., a "metal whose conductivity will not be lost even when the metal is oxidized", and the copper seed layer **111** are sequentially deposited over the bottoms and wall surfaces of the via hole **108** and the wiring trench **109**. Thereafter, by an electroplating process, the copper plating film **112** is grown on the copper seed layer **111** so as to completely fill the via hole **108** and the wiring trench **109**, and then the via **114** and second wiring **115** of the wiring copper film **113**, into which the copper seed layer **111** and the copper plating film **112** are integrated, are formed. Suppose that the second barrier metal film **110** and the copper seed layer **111** are sequentially deposited over the wall surfaces of the via hole **108** or the wiring trench **109**. In that case, even when the second barrier metal film **110** has exposed parts due to poor coverage of the copper seed layer **111**, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, this enables the formation of the copper plating film **112** on the copper seed layer **111** or over the second barrier metal film **110** in the via hole **108** or the wiring trench **109** by an electroplating process, while preventing generation of filling defects. As a result, a margin of filling the via hole **108** or the wiring trench **109** with the copper plating film **112** is increased.

Note that Ru is used as a material for the second barrier metal film **110** in the first embodiment; however, any other "metal whose conductivity will not be lost even when the metal is oxidized", e.g., Ir (specific resistance 6.5 $\mu\Omega \cdot$ cm: the specific resistance of IrO_2, which is an Ir oxide, is about 30 $\mu\Omega \cdot$ cm) or an alloy containing Ru or Ir, may alternatively be used.

Further, in the first embodiment, pure copper is used as a material for the first

wiring **103**, the copper seed layer **111** or the copper plating film **112**; however, a copper alloy may alternatively be used.

Furthermore, in the first embodiment, a Ta film is used as the first barrier metal film **102**; however, a TaN film, a Ti film, a TiN film or the like may alternatively be used.

In addition, in the first embodiment, an SiO_2 film, a coating film, a film which is deposited by a CVD process, includes C and has a low dielectric constant, or the like may be used as the first insulating film **101**, second insulating film **105** or third insulating film **107**.

Besides, a dual damascene process in which the via hole **108** and the wiring trench **109** are simultaneously filled with a conductive film is used in the first embodiment; however, the via hole **108** and the wiring trench **109** may alternatively be separately formed and then separately filled with a conductive film.

Moreover, in the first embodiment, in order to reduce the resistance of the first wiring **103** as well as the first barrier metal film **102** of a Ta film, some metal film other than a Ta film may be formed under the first barrier metal film **102**.

Also, in the first embodiment, in order to reduce the resistance of the via **114** or the second wiring **115** as well as the second barrier metal film **110** of a Ru film, some metal film other than a Ru film may be formed under the second barrier metal film **110**.

(Second Embodiment)

Hereinafter, a semiconductor device and a fabrication method thereof according to the second embodiment of the present invention will be described with reference to FIGS. **2(a)** through **2(e)**.

First, like the step shown in FIG. **1(a)** in the first embodiment, as shown in FIG. **2(a)**, a first wiring **203** of, e.g., a copper film, is embedded in a first insulating film **201** on

a semiconductor substrate **200** with a first barrier metal film **202** of, e.g., a Ta film, interposed therebetween. Thereafter, a first silicon nitride film **204**, a second insulating film **205**, a second silicon nitride film **206** and a third insulating film **207** are sequentially deposited over the semiconductor substrate **200**, and then a via hole **208** reaching the first wiring **203** and having a depth of about 500 nm is formed through the first silicon nitride film **204**, second insulating film **205** and second silicon nitride film **206**; in addition, a wiring trench **209** reaching the first wiring **203** through the via hole **208** and having a depth of about 300 nm is formed in the third insulating film **207**. In this case, the first barrier metal film **202** or the first silicon nitride film **204** prevents copper atoms constituting the first wiring **203** from diffusing into the first insulating film **201**, the second insulating film **205** or the like due to the thermal processing conducted at about 400°C (e.g., plasma CVD process) for the deposition of the second insulating film **205**, the second silicon nitride film **206** or the like. In other words, the first barrier metal film **202** or the first silicon nitride film **204** serves as a barrier against diffusion of the copper atoms.

Next, as shown in FIG. **2(b)**, a second barrier metal film **210** of a RuO_2 film is deposited to a thickness of 25 nm over the semiconductor substrate **100** by, e.g., a reactive sputtering process in which sputtering is carried out using Ru as sputtering targets in an atmosphere of oxygen (O_2), and then a copper seed layer **211** of a copper film is deposited to a thickness of 150 nm on the second barrier metal film **210** by, e.g., a sputtering process. Thus, the bottoms and wall surfaces of the via hole **208** and the wiring trench **209** are covered with the second barrier metal film **210** and the copper seed layer **211**.

The semiconductor substrate **200** is then transferred from the sputtering apparatus into a plating apparatus. At this time, if the second barrier metal film **210** has exposed parts due to poor coverage of the copper seed layer **211**, those parts will be exposed to the air. However, RuO_2 (specific resistance of 35 $\mu\Omega \cdot$ cm) constituting the second barrier

metal **210** is basically a conductive metal oxide and thus will not cause further oxidation to lose its conductivity.

Then, as shown in FIG. **2(c)**, a copper plating film **212** is grown to a thickness of 500 nm on the copper seed layer **211** by an electroplating process so as to completely fill the via hole **208** and the wiring trench **209**. More specifically, after the semiconductor substrate **200** has been immersed in a plating solution including $CuSO_4$, H_2SO_4 and the like, the electroplating process is conducted such that the semiconductor substrate **200** has a negative potential. At this time, even if the second barrier metal film **210** on wall surfaces of the via hole **208** or the like is not covered with the copper seed layer **211**, it can be avoided the conductivity of the second barrier metal film **210** will be lost due to oxidation thereof; thus, the via hole **208** and the wiring trench **209** can be reliably filled with the copper plating film **212**.

Thereafter, the semiconductor substrate **200** is removed from the plating apparatus, and then the copper plating film **212** is thermally processed (e.g., at a temperature of about 100°C for about two hours) in order to grow crystal grains of the copper plating film **212**. As a result, the copper seed layer **211** and the copper plating film **212** are integrated into a wiring copper film **213** as shown in FIG. **2(d)**. Note that, instead of thermally processing the copper plating film **212** as described above, the semiconductor substrate **200** may be left to stand at room temperature for about two days.

As shown in FIG. **2(e)**, by, e.g., a CMP process, parts of the second barrier metal film **210** and the wiring copper film **213** which are located outside the wiring trench **209** are then removed to form a via **214** and a second wiring **215** from the wiring copper film **213**. Thus, the first wiring **203** is connected to the second wiring **215** through the via **214**.

Although not shown, a desired multi-layer wiring structure is then formed as necessary by repeatedly conducting the steps shown in FIGS. **2(a)** through **2(e)** (regarding

FIG. 2(a), the step of depositing the first silicon nitride film **204** and the subsequent steps).

As described above, according to the second embodiment, the second barrier metal film **210** of RuO_2, i.e., a "conductive metal oxide", and the copper seed layer **211** are sequentially deposited over the bottoms and wall surfaces of the via hole **208** and the wiring trench **209**. Thereafter, by an electroplating process, the copper plating film **212** is grown on the copper seed layer **211** so as to completely fill the via hole **208** and the wiring trench **209**, and then the via **214** and second wiring **215** of the wiring copper film **213**, into which the copper seed layer **211** and the copper plating film **212** are integrated, are formed. Suppose that the second barrier metal film **210** and the copper seed layer **211** are sequentially deposited over the wall surface of the via hole **208** or wiring trench **209**. In that case, even when the second barrier metal film **210** has exposed parts due to poor coverage of the copper seed layer **211**, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, this enables the formation of the copper plating film **212** on the copper seed layer **211** or over the second barrier metal film **210** in the via hole **208** or the wiring trench **209** by an electroplating process, while preventing generation of filling defects. As a result, a margin of filling the via hole **208** or the wiring trench **209** with the copper plating film **212** is increased.

Note that, in the second embodiment, RuO_2 is used as a material for the second barrier metal film **210**; however, any other "conductive metal oxide", e.g., IrO_2 (specific resistance of about 30 $\mu\Omega \cdot$ cm), an alloy oxide containing Ru or Ir, a superconducting oxide such as YBCO ($YBa_2Cu_3O_{7-x}$), or a compound such as $La_{0.8}Sr_{0.2}MnO_3$, may alternatively be used.

Further, in the second embodiment, pure copper is used as a material for the first wiring **203**, the copper seed layer **211** or the copper plating film **212**; however, a copper alloy may alternatively be used.

Furthermore, in the second embodiment, a Ta film is used as the first barrier metal film **202**; however, a TaN film, a Ti film, a TiN film or the like may alternatively be used.

In addition, in the second embodiment, an SiO_2 film, a coating film, a CVD film including C and having a low dielectric constant, or the like may be used as the first insulating film **201**, second insulating film **205** or third insulating film **207**.

Besides, a dual damascene process in which the via hole **208** and the wiring trench **209** are simultaneously filled with a conductive film is used in the second embodiment; however, the via hole **208** and the wiring trench **209** may alternatively be separately formed and separately filled with a conductive film.

Moreover, in the second embodiment, in order to reduce the resistance of the first wiring **203** as well as the first barrier metal film **202** of a Ta film, some metal film other than a Ta film may be formed under the first barrier metal film **202**.

Also, in the second embodiment, in order to reduce the resistance of the via **214** or the second wiring **215** as well as the second barrier metal film **210** of a RuO_2 film, some metal film other than a RuO_2 film may be formed under the second barrier metal film **210**.

(Third Embodiment)

Hereinafter, a semiconductor device and a fabrication method thereof according to the third embodiment of the present invention will be described with reference to FIGS. **3(a)** through **3(d)**.

First, like the step shown in FIG. **1(a)** in the first embodiment, as shown in FIG. **3(a)**, a first wiring **303** of, e.g., a copper film, is embedded in a first insulating film **301** on a semiconductor substrate **300** with a first barrier metal film **302** of, e.g., a Ta film, interposed therebetween. Thereafter, a first silicon nitride film **304**, a second insulating film **305**, a second silicon nitride film **306** and a third insulating film **307** are sequentially

deposited over the semiconductor substrate **300**, and then a via hole **308** reaching the first wiring **303** and having a depth of about 500 nm is formed through the first silicon nitride film **304**, second insulating film **305** and second silicon nitride film **306**; in addition, a wiring trench **309** reaching the first wiring **303** through the via hole **308** and having a depth of about 300 nm is formed in the third insulating film **307**. In this case, the first barrier metal film **302** or the first silicon nitride film **304** prevents copper atoms constituting the first wiring **303** from diffusing into the first insulating film **301**, the second insulating film **305** or the like due to the thermal processing conducted at about 400°C (e.g., plasma CVD process) for the deposition of the second insulating film **305**, the second silicon nitride film **306** or the like. In other words, the first barrier metal film **302** or the first silicon nitride film **304** serves as a barrier against diffusion of the copper atoms.

As shown in FIG. **3(b)**, a second barrier metal film **310** of, e.g., a Ru film, is then deposited to a thickness of 25 nm over the semiconductor substrate **300** by, e.g., a sputtering process. Accordingly, the bottoms and wall surfaces of the via hole **308** and the wiring trench **309** are covered with the second barrier metal film **310**. Thereafter, a wiring copper film **311** is deposited to a thickness of 600 nm on the second barrier metal film **310** by, e.g., a sputtering process. At this time, the via hole **308** or the wiring trench **309** cannot be filled with the wiring copper film **311** due to the directivity of the sputtering process, as shown in FIG. **3(b)**.

As shown in FIG. **3(c)**, the wiring copper film **311** is then repeatedly oxidized and reduced in an oxidative-reducing atmosphere by, e.g., an oxidation-reduction reflow process, and the resultant reaction heat causes the wiring copper film **311** to flow, thereby filling the via hole **308** and the wiring trench **309**. Note that, when the wiring copper film **311** is oxidized, the second barrier metal **310** is also oxidized. However, the specific resistance of Ru constituting the second barrier metal film **310** is 7.5 $\mu\Omega \cdot$ cm, while the

specific resistance of RuO_2, which is a Ru oxide, is 35 μΩ • cm; therefore, the second barrier metal film **310** will not lose its conductivity when oxidized.

As shown in FIG. **3(d)**, by, e.g., a CMP process, parts of the second barrier metal film **310** and the wiring copper film **311** which are located outside the wiring trench **309** are then removed to form a via **312** and a second wiring **313** from the wiring copper film **311**. Thus, the first wiring **303** is connected to the second wiring **313** through the via **312**.

Although not shown, a desired multi-layer wiring structure is then formed as necessary by repeatedly conducting the steps shown in FIGS. **3(a)** through **3(d)** (regarding FIG. **3(a)**, the step of depositing the first silicon nitride film **304** and the subsequent steps).

As described above, according to the third embodiment, the second barrier metal film **310** of Ru, i.e., a "metal whose conductivity will not be lost even when the metal is oxidized", is deposited on the bottoms and wall surfaces of the via hole **308** and the wiring trench **309**, and then the wiring copper film **311** is formed on the second barrier metal film **310** so as to completely fill the via hole **308** and the wiring trench **309**, thereby forming the via **312** and the second wiring **313**. Accordingly, even when the second barrier metal film **310** is deposited on the wall surfaces of the via hole **308** or the wiring trench **309** and then the wiring copper film **311** is formed on the second barrier metal film **310**, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the second barrier metal film **310** will not be lost due to the oxidation thereof. Thus, the resistance of the via **312** or the second wiring **313** as well as the second barrier metal film **310** can be prevented from increasing due to the oxidation of the second barrier metal film **310**.

Note that, in the third embodiment, Ru is used as a material for the second barrier metal film **310**; however, any other "metal whose conductivity will not be lost even when the metal is oxidized", e.g., Ir or an alloy containing Ru or Ir, may alternatively be used. Also, instead of a "metal whose conductivity will not be lost even when the metal is

oxidized", a "conductive metal oxide", e.g., RuO_2, IrO_2, an alloy oxide containing Ru or Ir, a superconducting oxide such as YBCO, or a compound such as $La_{0.8}Sr_{0.2}MnO_3$, may alternatively be used.

Further, in the third embodiment, pure copper is used as a material for the first wiring **303** or the wiring copper film **311**; however, a copper alloy may alternatively be used.

Furthermore, in the third embodiment, a Ta film is used as the first barrier metal film **302**; however, a TaN film, a Ti film, a TiN film or the like may alternatively be used.

In addition, in the third embodiment, an SiO_2 film, a coating film, a CVD film including C and having a low dielectric constant, or the like may be used as the first insulating film **301**, second insulating film **305** or third insulating film **307**.

Besides, in the third embodiment, in order to form the wiring copper film **311**, a combination of sputtering and reflow processes is used; however, a CVD process, an electroless plating process, an ion plating process, a combination of CVD and high-temperature sputtering processes (a process in which after a thin copper film has been deposited by a CVD process, a thick copper film is deposited on the thin copper film by a high-temperature sputtering process) or the like may alternatively be used. Also, although an oxidative-reducing reflow process is used as the reflow process in the combination of sputtering and reflow processes, some other reflow process may alternatively be used.

Moreover, a dual damascene process in which the via hole **308** and the wiring trench **309** are simultaneously filled with a conductive film is used in the third embodiment; however, the via hole **308** and the wiring trench **309** may alternatively be separately formed and separately filled with a conductive film.

Also, in the third embodiment, in order to reduce the resistance of the first wiring **303** as well as the first barrier metal film **302** of a Ta film, some metal film other than a Ta

film may be formed under the first barrier metal film **302**.

Furthermore, in the third embodiment, in order to reduce the resistance of the via **312** or the second wiring **313** as well as the second barrier metal film **310** of a Ru film, some metal film other than a Ru film may be formed under the second barrier metal film **310**.

(Fourth Embodiment)

Hereinafter, a semiconductor device and a fabrication method thereof according to the fourth embodiment of the present invention will be described with reference to FIGS. **4(a)** through **4(e)** and FIGS. **5(a)** through **5(d)**.

First, as shown in FIG. **4(a)**, a first barrier metal film **402** of a Ru film is deposited to a thickness of 10 nm on a first insulating film **401** overlying a semiconductor substrate **400** by, e.g., a sputtering process, and then a copper seed layer **403** of a copper film is deposited to a thickness of 100 nm on the first barrier metal film **402** by, e.g., a sputtering process.

The semiconductor substrate **400** is then transferred from the sputtering apparatus into a plating apparatus. At this time, if the first barrier metal film **402** has exposed parts due to the poor coverage of the copper seed layer **403**, those parts will be exposed to the air and therefore oxidized. However, the specific resistance of Ru constituting the first barrier metal film **402** is 7.5 $\mu\Omega \cdot$ cm, while the specific resistance of RuO_2, which is a Ru oxide, is 35 $\mu\Omega \cdot$ cm; therefore, even when the first barrier metal film **402** is oxidized, the conductivity thereof will not be lost.

Then, as shown in FIG. **4(a)**, a copper plating film **404** is grown to a thickness of 500 nm on the copper seed layer **403** by an electroplating process. More specifically, after the semiconductor substrate **400** has been immersed in a plating solution including $CuSO_4$,

H_2SO_4 and the like, the electroplating process is conducted such that the semiconductor substrate **400** has a negative potential. Note that, although not shown, in the case where the first insulating film **401** has a recess such as a contact hole or via hole, the recess is filled with the copper plating film **404** with the first barrier metal film **402** and the copper seed layer **403** interposed therebetween.

Thereafter, the semiconductor substrate **400** is removed from the plating apparatus, and then the copper plating film **404** is thermally processed (e.g., at a temperature of about 100°C for about two hours) in order to grow crystal grains of the copper plating film **404**. As a result, the copper seed layer **403** and the copper plating film **404** are integrated into a first wiring copper film **405**, as shown in FIG. **4(b)**. Note that, instead of thermally processing the copper plating film **404** as described above, the semiconductor substrate **400** may be left to stand at room temperature for about two days.

As shown in FIG. **4(b)**, a first resist pattern **406** is then formed on the first wiring copper film **405** so as to cover a first wiring forming region.

Next, by using the first resist pattern **406** as a mask, the first wiring copper film **405** and the first barrier metal film **402** are sequentially etched to form a first wiring **407** over the first insulating film **401** with the first barrier metal film **402** interposed therebetween, as shown in FIG. **4(c)**.

Thereafter, as shown in FIG. **4(d)**, a silicon nitride film **408** and a second insulating film **409** are sequentially deposited over the first insulating film **401** as well as the first wiring **407**. As a result, the top and side surfaces of the first wiring **407** are covered with the second insulating film **409** with the silicon nitride film **408** interposed therebetween. In this case, the first barrier metal film **402** or the silicon nitride film **408** prevents copper atoms constituting the first wiring **407** from diffusing into the first insulating film **401**, the second insulating film **409** or the like due to the thermal processing conducted at about

400°C (e.g., plasma CVD process) for the deposition of the second insulating film **409** or the like. In other words, the first barrier metal film **402** or the silicon nitride film **408** serves as a barrier against diffusion of the copper atoms.

As shown in FIG. **4(e)**, a via hole **410** reaching the first wiring **407** and having a depth of about 500 nm is then formed through the silicon nitride film **408** and the second insulating film **409**.

As shown in FIG. **5(a)**, a second barrier metal film **411** of a Ru film is then deposited to a thickness of 25 nm on the second insulating film **409** as well as in the via hole **410** by, e.g., a sputtering process. Thus, the bottom and wall surface of the via hole **410** are covered with the second barrier metal film **411**.

Thereafter, a second wiring copper film **412** is deposited to a thickness of 600 nm on the second barrier metal film **411** by, e.g., a sputtering process. At this time, the via hole **410** cannot be filled with the second wiring copper film **412** due to the directivity of the sputtering process, as shown in FIG. **5(a)**.

As shown in FIG. **5(b)**, the second wiring copper film **412** is then repeatedly oxidized and reduced in an oxidative-reducing atmosphere by, e.g., an oxidation-reduction reflow process, and the resultant reaction heat causes the second wiring copper film **412** to flow, thereby filling the via hole **410**. Note that, when the second wiring copper film **412** is oxidized, the second barrier metal film **411** is also oxidized. However, the specific resistance of Ru constituting the second barrier metal film **411** is 7.5 $\mu\Omega \cdot$ cm, while the specific resistance of RuO_2, which is a Ru oxide, is 35 $\mu\Omega \cdot$ cm; therefore, even when the second barrier metal film **411** is oxidized, the conductivity thereof will not be lost.

As shown in FIG. **5(c)**, a second resist pattern **413** is then formed on the second wiring copper film **412** so as to cover a second wiring forming region. Thereafter, by using the second resist pattern **413** as a mask, the second wiring copper film **412** and the

second barrier metal film **411** are sequentially etched to form a via **414** and a second wiring **415** from the second wiring copper film **412**, as shown in FIG. **5(d)**. Thus, the first wiring **407** is connected to the second wiring **415** through the via **414**.

Although not shown, a desired multi-layer wiring structure is then formed as necessary by repeatedly conducting the steps shown in FIGS. **4(d)** and **4(e)**, and FIGS. **5(a)** through **5(d)**.

As described above, according to the fourth embodiment, the first barrier metal film **402** of Ru, i.e., a "metal whose conductivity will not be lost even when the metal is oxidized," and the copper seed layer **403** are sequentially deposited over the first insulating film **401**. Thereafter, by an electroplating process, the copper plating film **404** is grown on the copper seed layer **403**, and then the first wiring copper film **405**, into which the copper seed layer **403** and the copper plating film **404** are integrated, is etched to form the first wiring **407**. Suppose that the first barrier metal film **402** and the copper seed layer **403** are sequentially deposited over the first insulating film **401**. In that case, even when the first barrier metal film **402** has exposed parts due to poor coverage of the copper seed layer **403**, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, the resistance of the first wiring **407** as well as the first barrier metal film **402** can be prevented from increasing due to the oxidation of the first barrier metal film **402**.

Furthermore, according to the fourth embodiment, the second barrier metal film **411** of Ru, i.e., a "metal whose conductivity will not be lost even when the metal is oxidized," is deposited on the second insulating film **409** as well as in the via hole **410**. Thereafter, the second wiring copper film **412** is formed on the second barrier metal film **411** so as to completely fill the via hole **410**, and then the second wiring copper film **412** is etched to form the via **414** and the second wiring **415**. Thus, even when the second barrier

metal film **411** is deposited on the second insulating film **409** and then the second wiring copper film **412** is formed on the second barrier metal film **411**, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the second barrier metal film **411** will be lost due to the oxidation thereof. Therefore, the resistance of the via **414** or the second wiring **415** as well as the second barrier metal film **411** can be prevented from increasing due to the oxidation of the second barrier metal film **411**.

Note that, in the fourth embodiment, Ru is used as a material for the first barrier metal film **402** or the second barrier metal film **411**; however, any other "metal whose conductivity will not be lost even when the metal is oxidized", e.g., Ir or an alloy containing Ru or Ir, may alternatively be used. Also, instead of a "metal whose conductivity will not be lost even when the metal is oxidized", a "conductive metal oxide", e.g., RuO_2, IrO_2, an alloy oxide containing Ru or Ir, a superconducting oxide such as YBCO, or a compound such as $La_{0.8}Sr_{0.2}MnO_3$, may alternatively be used.

In addition, in the fourth embodiment, pure copper is used as a material for the copper seed layer **403**, the copper plating film **404** or the second wiring copper film **412**; however, a copper alloy may alternatively be used.

Besides, in the fourth embodiment, an SiO_2 film, a coating film, a CVD film including C and having a low dielectric constant, or the like may be used as the first insulating film **401** or second insulating film **409**.

Further, in the fourth embodiment, in order to form the second wiring copper film **412**, the combination of sputtering and reflow processes is used; however, a CVD process, an electroless plating process, an ion plating process, a combination of CVD and high-temperature sputtering processes or the like may alternatively be used. Also, although an oxidative-reducing reflow process is used as the reflow process in the combination of sputtering and reflow processes, some other reflow process may alternatively be used.

Furthermore, in the fourth embodiment, in order to reduce the resistance of the first wiring **407** as well as the first barrier metal film **402** of a Ru film, some metal film other than a Ru film may be formed under the first barrier metal film **402**.

Moreover, in the fourth embodiment, in order to reduce the resistance of the via **414** or the second wiring **415** as well as the second barrier metal film **411** of a Ru film, some metal film other than a Ru film may be formed under the second barrier metal film **411**.

[Effects of the Invention]

According to the present invention, even if a barrier metal film has exposed parts due to poor coverage of a seed layer when the barrier metal film and seed layer have been sequentially deposited over wall surfaces of a recess, it is avoided that the conductivity of the exposed parts will be lost due to the oxidation thereof. Therefore, this enables the formation of a conductive film on the seed layer or over the barrier metal film located in the recess by an electroplating process, while preventing generation of filling defects.

Furthermore, according to the present invention, even when a conductive film for wiring is formed on a barrier metal film, e.g., in an oxidative atmosphere, it is avoided that the conductivity of the barrier metal film will be lost due to the oxidation thereof. Thus, wiring resistance can be prevented from increasing due to the oxidation of the barrier metal film.

[Brief Description of the Drawings]

[FIG. 1]

(a) through (e) are cross-sectional views illustrating respective steps of a method for fabricating a semiconductor device according to a first embodiment of the present invention.

[FIG. 2]

(a) through (e) are cross-sectional views illustrating respective steps of a method for fabricating a semiconductor device according to a second embodiment of the present invention.

[FIG. 3]

(a) through (d) are cross-sectional views illustrating respective steps of a method for fabricating a semiconductor device according to a third embodiment of the present invention.

[FIG. 4]

(a) through (e) are cross-sectional views illustrating respective steps of a method for fabricating a semiconductor device according to a fourth embodiment of the present invention.

[FIG. 5]

(a) through (d) are cross-sectional views illustrating respective steps of the method for fabricating a semiconductor device according to the fourth embodiment of the present invention.

[FIG. 6]

(a) through (e) are cross-sectional views illustrating respective steps of a conventional method for fabricating a semiconductor device.

[FIG. 7]

(a) and (b) are diagrams for describing problems of the conventional method for fabricating a semiconductor device.

[Description of the Reference Characters]

100 semiconductor substrate

101 first insulating film

102 first barrier metal film

103 first wiring

104 first silicon nitride film

105 second insulating film

106 second silicon nitride film

107 third insulating film

108 via hole

109 wiring trench

110 second barrier metal film

111 copper seed layer

112 copper plating film

113 wiring copper film

114 via

115 second wiring

200 semiconductor substrate

201 first insulating film

202 first barrier metal film

203 first wiring

204 first silicon nitride film

205 second insulating film

206 second silicon nitride film

207 third insulating film

208 via hole

209 wiring trench

210 second barrier metal film

211 copper seed layer

212 copper plating film

213 wiring copper film

214 via

215 second wiring

300 semiconductor substrate

301 first insulating film

302 first barrier metal film

303 first wiring

304 first silicon nitride film

305 second insulating film

306 second silicon nitride film

307 third insulating film

308 via hole

309 wiring trench

310 second barrier metal film

311 wiring copper film

312 via

313 wiring

400 semiconductor substrate

401 first insulating film

402 first barrier metal film

403 copper seed layer

404 copper plating film

405 first wiring copper film

406 first resist pattern

407 first wiring

408 silicon nitride film

409 second insulating film

410 via hole

411 second barrier metal film

412 second wiring copper film

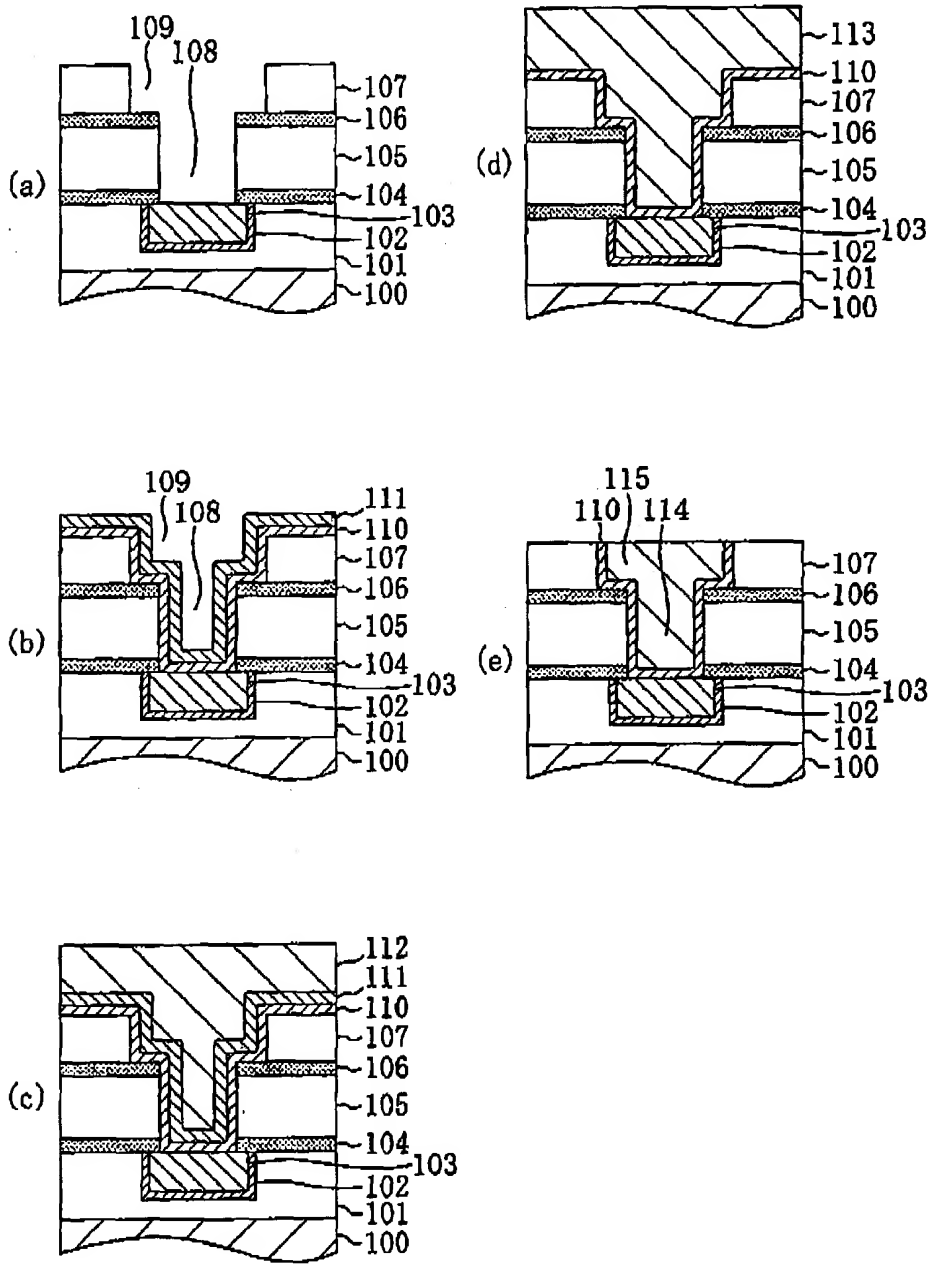
413 second resist pattern

414 via

415 second wiring

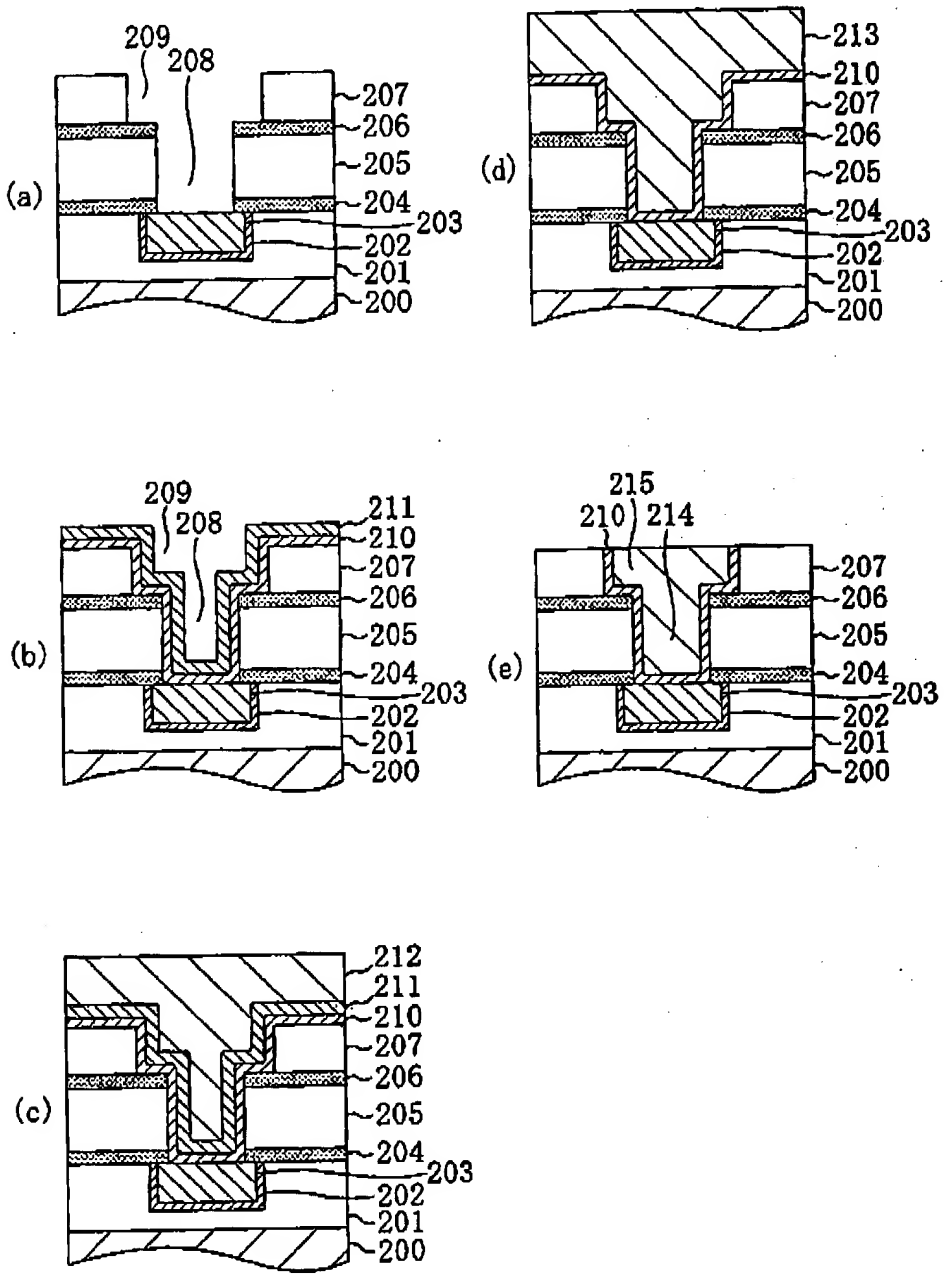
提出日 平成１２年 ８月２４日
整理番号＝２９２６４１０２４５ 頁: 1/ 7

【書類名】 図面→ Drawings
↳ Name of the Document
【図１】
↓
FIG. 1



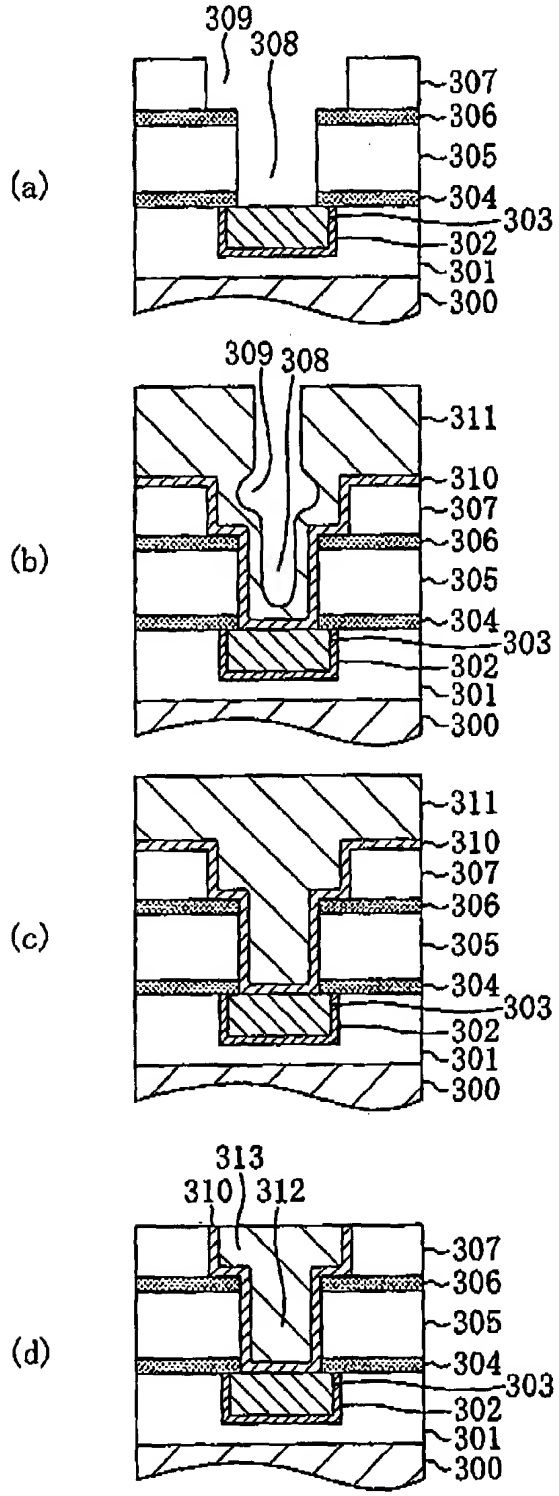
【図２】

FIG. 2


(a)
209
208
207
206
205
204
203
202
201
200
(d)
213
210
207
206
205
204
203
202
201
200
(b)
209
208
211
210
207
206
205
204
203
202
201
200
(e)
215
210
214
207
206
205
204
203
202
201
200
(c)
212
211
210
207
206
205
204
203
202
201
200

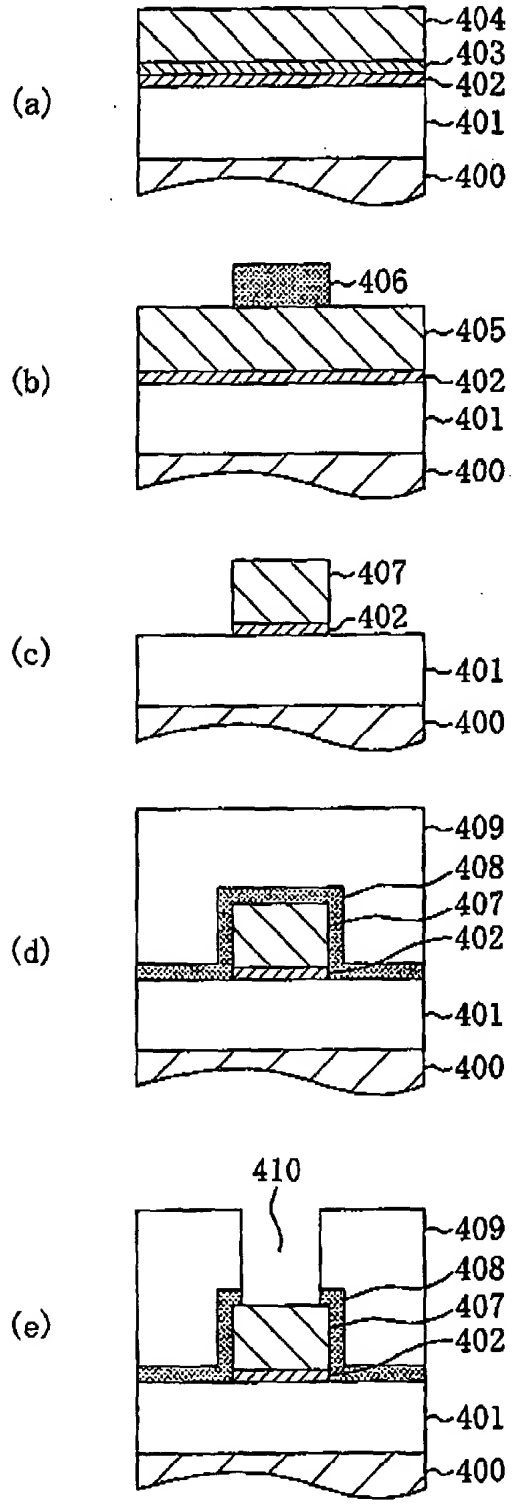
【図3】

FIG. 3


(a)
309
308
307
306
305
304
303
302
301
300
(b)
309
308
311
310
307
306
305
304
303
302
301
300
(c)
311
310
307
306
305
304
303
302
301
300
(d)
313
310
312
307
306
305
304
303
302
301
300

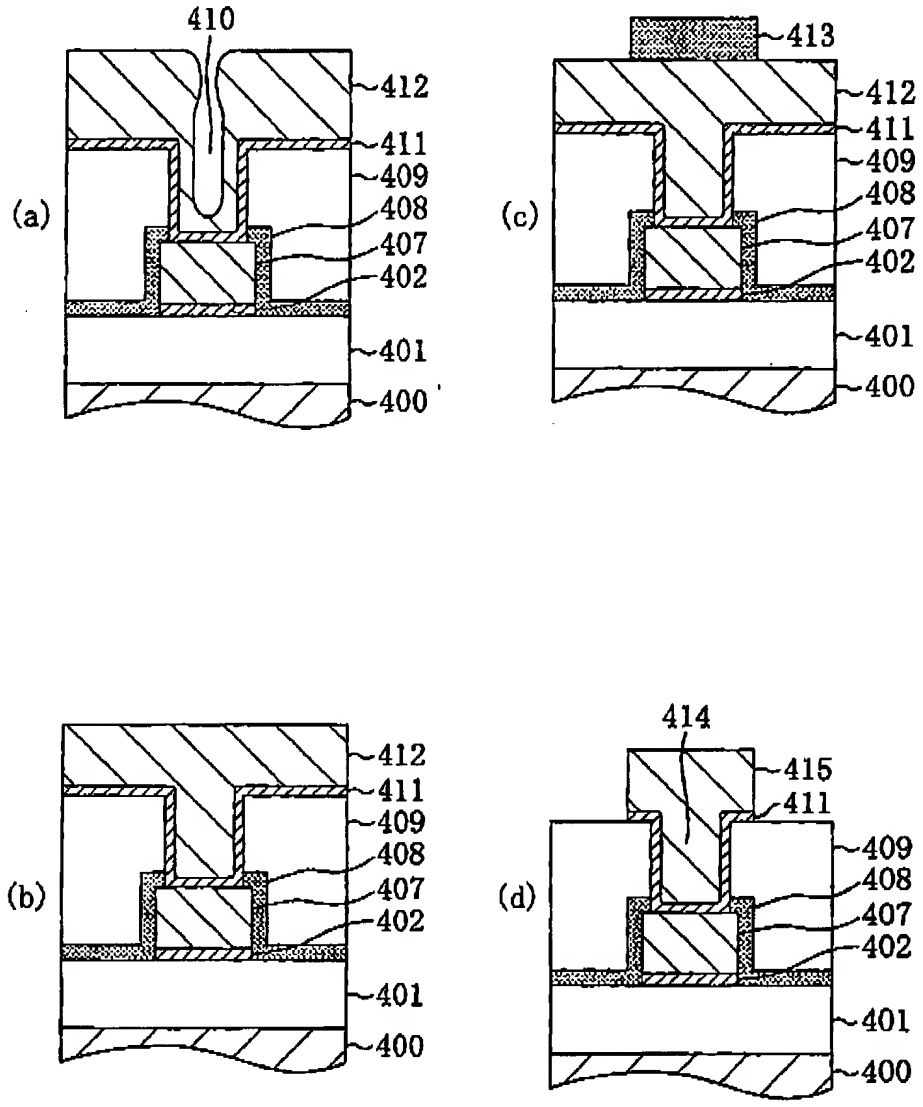
【図４】

FIG. 4


(a)
404
403
402
401
400
(b)
406
405
402
401
400
(c)
407
402
401
400
(d)
409
408
407
402
401
400
(e)
410
409
408
407
402
401
400

【図５】

FIG. 5


(a)
410
412
411
409
408
407
402
401
400
(c)
413
412
411
409
408
407
402
401
400
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402
401
400
(d)
414
415
411
409
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407
402
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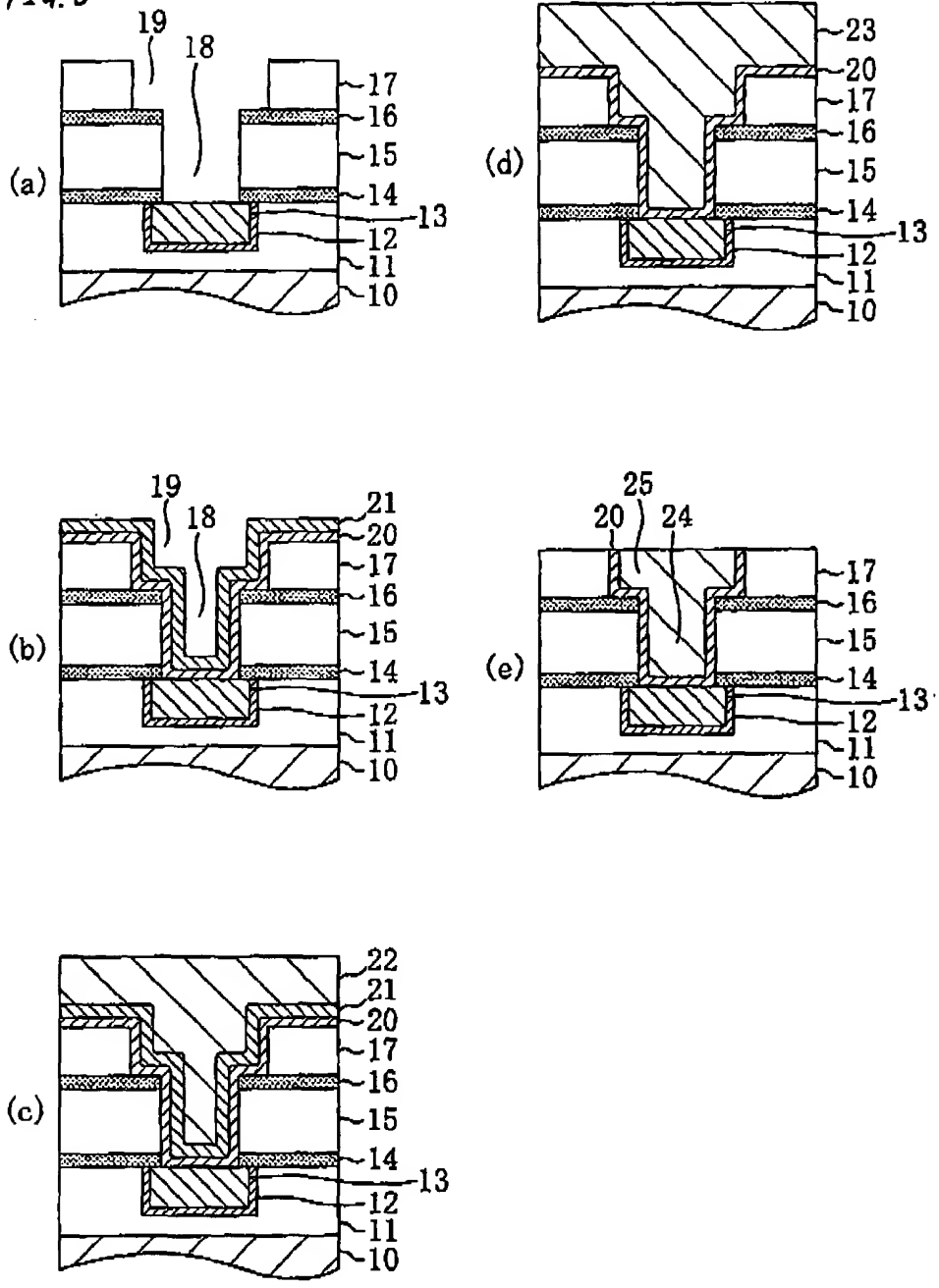
【図６】

FIG. 6


(a)
19
18
17
16
15
14
13
12
11
10
(d)
23
20
17
16
15
14
13
12
11
10
(b)
19
18
21
20
17
16
15
14
13
12
11
10
(e)
25
20
24
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16
15
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22
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13
12
11
10

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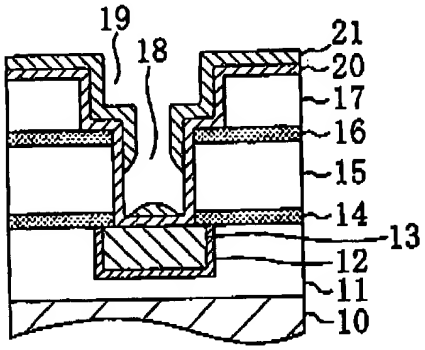
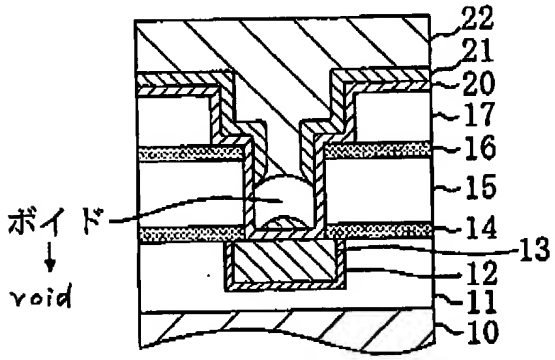
【図７】

FIG.7

(a)



(b)



[Name of the Document] Abstract

[Abstract]

[Problem] To enable a conductive film to be formed on a seed layer or over a barrier metal film in a recess by an electroplating process, while preventing generation of filling defects.

[Solution] A via hole **108** and a wiring trench **109** are formed in insulating films over a semiconductor substrate **100**, and then a second barrier metal film **110** of a Ru film, and a copper seed layer **111** are sequentially deposited over the bottoms and wall surfaces of the via hole **108** and the wiring trench **109**. A copper plating film **112** is grown on the copper seed layer **111** by an electroplating process so as to completely fill the via hole **108** and the wiring trench **109**. The copper seed layer **111** and the copper plating film **112** are integrated into a wiring copper film **113**, and then a via **114** and a second wiring **115** which are formed of the wiring copper film **113** are provided.

[Selected Figure] FIG. **1**